Amendments to the Claims:

This listing of claims will replace all prior versions, and listings of claims in the application:

Listing of Claims:

1. (Currently amended) A method ~~for loading pixels into a temporary memory,~~ comprising:

~~loading~~ retrieving a block of pixels associated with a reference block from a reference frame memory; wherein said block of pixels includes NxM pixels wherein N represents the number of pixels in each row of the reference block and wherein M represents the number of pixels in each column of the reference block; and ~~into said temporary memory~~;

~~loading~~ storing said NxM pixels in a staging memory wherein said NxM pixels are rearranged and stored in the staging memory so as to form P groups each having L pixels such that during each read access cycle all L pixels of a different one of the P groups is read from the staging memory to a temporary memory; wherein each group of L pixels corresponds to a new row or a new column of said block of pixels ~~with pixels for updating said block of pixels, by rearranging said pixels so that an update group of pixels can be accessed in parallel from said staging memory~~ ;

~~updating said block of pixels in said temporary memory with an update group of pixels from said staging memory in parallel.~~

2. (Currently amended) The method of claim 1 wherein said temporary memory is ~~connected~~ coupled to a processing unit for comparing said block of pixels to a second block of pixels.

3. Canceled.

4. (Original) The method of claim 2 wherein said processing unit performs a comparison for a motion estimation algorithm.

5. (Currently amended) The method of claim 1 wherein said staging memory comprises banks of memories, each bank providing a different one ~~of said update~~ P group of pixels.

6. (Currently amended) The method of claim 5 wherein ~~said update group of pixels~~ the L pixels of each group is one of a row and column of rearranged pixels.

7. (Currently amended) The method of claim 1 further comprising providing a search pattern that can be executed by loading said temporary memory, in a single cycle, with pixels to provide a next block to be searched.

8. (Currently amended) The method of claim 7 wherein said search pattern is one of a spiral, horizontal and vertical search pattern.

9. (Original) The method of claim 1 wherein said rearranging of said pixels comprises reordering said pixels in each row so that each pixels from a single column are spread across a plurality of columns so that they can be accessed in parallel.

10. Canceled.

11. Canceled.

12. (Currently amended) An apparatus ~~for loading pixels into a temporary memory,~~ comprising:

a ~~temporary~~ reference frame memory for storing and supplying a block of pixels associated with a reference block from a reference frame memory; wherein said block of pixels includes NxM pixels wherein N represents the number of pixels in each row of the reference block and wherein M represents the number of pixels in each column of the reference block; and;

a staging memory for storing ~~new pixels for updating said block of pixels~~ said NxM pixels; and

an address translator for rearranging said ~~new pixels so that an update group of said new pixels can be accessed in parallel from said staging memory~~ NxM pixels so as to form

P groups each having L pixels such that during each read access cycle all L pixels of a different one of the P groups is read from the staging memory to a temporary memory; wherein each group of L pixels corresponds to a new row or a new column of said block of pixels;

an addressing unit for providing a block of pixels in parallel from said staging memory to said temporary memory.

13. Canceled.

14. (Currently amended) The apparatus of claim 12 wherein said staging memory comprises a plurality of memory banks each bank providing a different one of said P groups.

15. (Original) The apparatus of claim 12 wherein said staging memory comprises SRAM memory.

16. (Currently amended) The apparatus of claim 12 wherein said temporary memory is a two-dimensional shift register, and wherein the L pixels in each of the P groups ~~said update group of pixels~~ corresponds to a ~~shifted~~ new row or column of said block of ~~data~~ pixels.

17. (Currently amended) The apparatus of claim 12 wherein said temporary memory is ~~connected~~ coupled to a processing unit for comparing said block of pixels to a second block of pixels.

18. (Currently amended) The apparatus of claim 17 wherein said processing unit performs a comparison for a motion estimation algorithm.

19. Canceled.

20. (Currently amended) The apparatus of claim ~~19~~ 16 further comprising:

~~four~~ a plurality of buffers coupled to said two dimensional shift register for buffering new rows and columns of pixels to be shifted in from the left, right, top and bottom.